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DF1508

Power Management IC with LNB Supply & Control

GERNAL DESCRIPTION

DF1508 is a highly integrated power management IC (PMIC) designed for analog and digital satellite receivers such as ABS-S, DVB-S/S2 and consumer and multimedia applications with DVB-S2.
Providing a complete system power management solution specifically to provide the 14.4V to 19.4V power supply to the LNB down converter in the antenna dish or to the multi switch box. It offers a complete solution with minimum component count, low power dissipation together with simple design. the DF1508 integrates 1-CH LNB power supply and control voltage converter, 4- CH synchronous buck converter, 2- CH LDO， 1- CH reset monitor. The converters are optimized for high efficiency (greater than 92%) and feature integrated low impedance FETs.

FEATURES

- Wide Input Voltage Range: 3.4V ~ 20V
  High Efficient DC/DC Converter：92~96%
  Low Power Consumption (Sleep Mode) < 10μA
  Integrate 8-CH Output in QFN40L-5X5 Package
- LNB Supply and Control (1-CH)
  BOOST: output 14.4V/19.4V, load current up to 600mA; low noise single output
- Buck DC/DC Converter (4-CH)
  HVBUCK1: Input 3.4V~20V, output 0.6V ~ VIN adjustable, load current up to 3A
  HVBUCK2: Input 3.4V~20V, output 0.6V~ VIN adjustable, load current up to 3A
  LVBUCK1: Input 2.5V~6V, output 0.6V~ VIN adjustable, load current up to 3A
  LVBUCK2: Input 2.5V~6V, output 0.6V~ VIN adjustable, load current up to 3A
- High PSRR LDO (2-CH)
  LDO1:3.3V fixed output voltage, load current up to 800mA.
  LDO2:0.6V~5.0V adjustable, load current up to 1000mA.
- Reset Monitor (1-CH)
  provide a reset signal POR to the host processor with an external pull up voltage
- Protection
  Over Voltage Protection (OVP)
  Under Voltage Protection (UVP)
  Over current protection (OCP)
  Short circuit protection (SCP)
  Over thermal protection (OTP)

APPLICATION

- DVB-S2
- ABS-S
- OTT+DVB-S2

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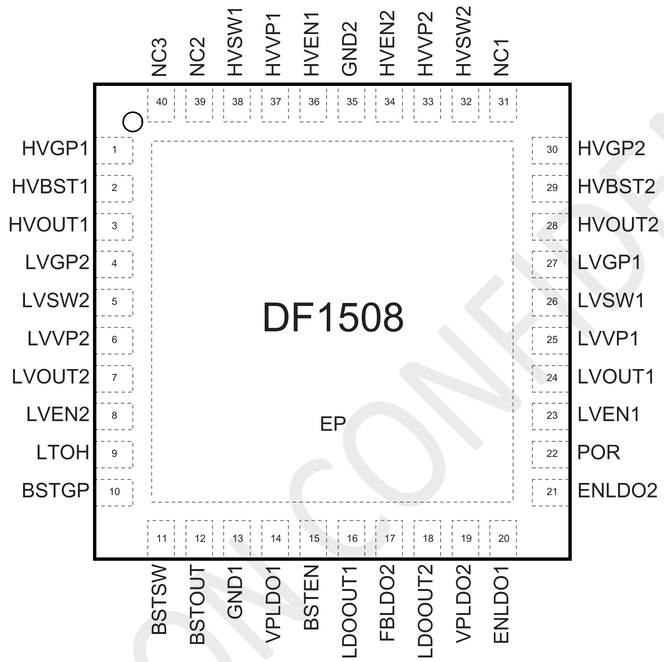
PRODUCT OPTIONS

BLOCK	INPUT VOLTAGE	OUTPUT VOLTAGE	CAPABILITY
HVBUCK1/HVBUCK2	3.4~20V	Adjustable	Up to 3A
LVBUCK1/LVBUCK2	2.5~6V	Adjustable	Up to 3A
LNB BOOST	2.5~20V	14.4V/19.4V	Up to 600mA
LDO1	2.5V~6V	Fixed 3.3V	Up to 800mA
LDO2	2.5V~6V	Adjustable	Up to 1000mA
RESET MONITOR	HVOUT2	External pull up voltage	100mS delay for Processor

PIN CONFIGURATION

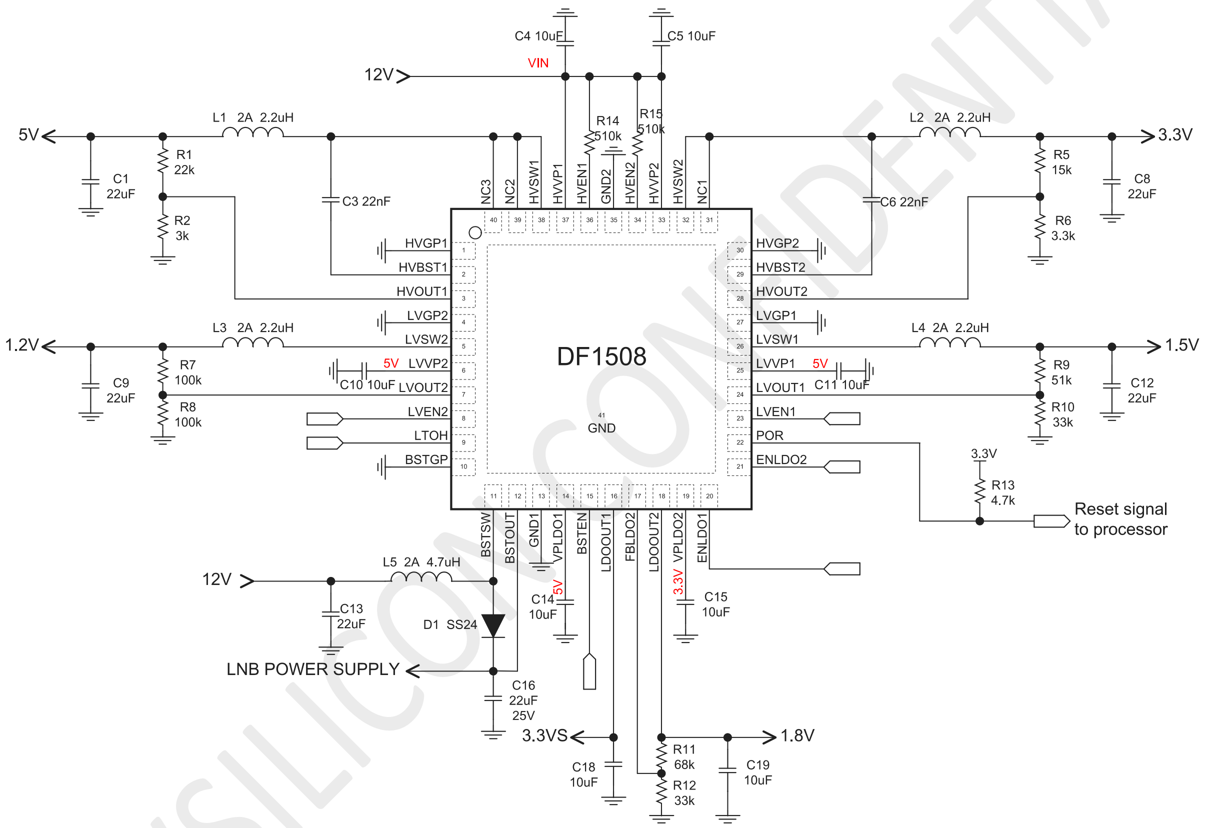


PIN DESCRIPTIONS

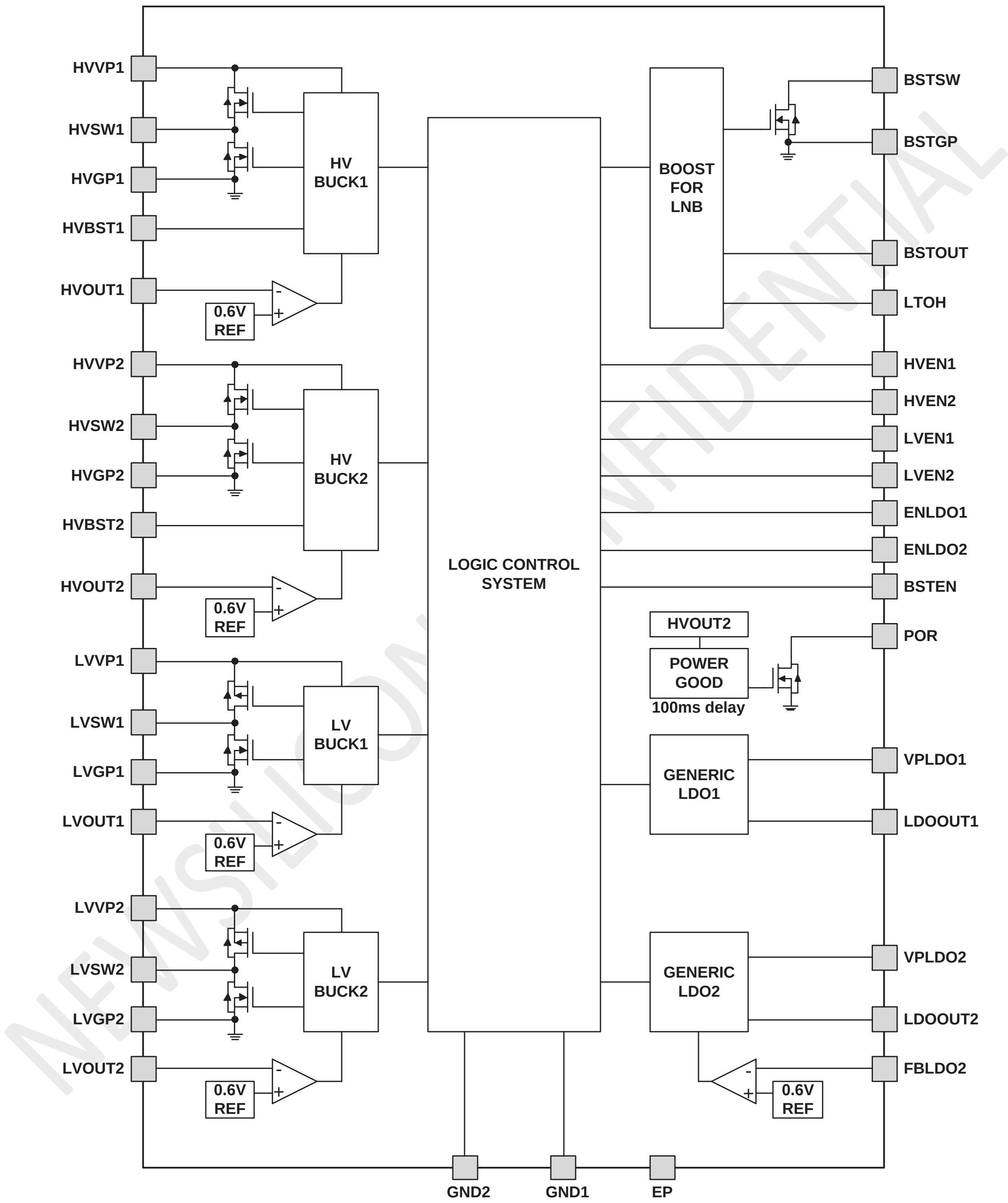
PIN	NAME	DESCRIPTION
1	HVGP1	Ground
2	HVBST1	Bootstrap. A capacitor connected between HVSW1 and HVBST1 pins is required to form a floating supply across the high-side switch driver. Use a 22nF capacitor
3	HVOUT1	HVBUCK1 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
4	LVGP2	Ground
5	LVSW2	LVBUCK2 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
6	LVVP2	LVBUCK2 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
7	LVOUT2	LVBUCK2 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
8	LVEN2	LVBUCK2 Enable (Active High) or Disable(Low or Floating).
9	LTOH	LNB 14.4V/19.4V Switch, LTOH=LOW(14.4V), LTOH=HIGH(19.4V),
10	BSTGP	Ground
11	BSTSW	BOOST Switching Pin, Connect this Pin to inductor and catch diode, Minimize the track area to reduce EMI.
12	BSTOUT	BOOST Feedback. Connect to the output.
13	GND1	Ground

14	VPLDO1	LDO1 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
15	BSTEN	BOOST Enable (Active High) or Disable(Low or Floating).
16	LDOOUT1	LDO1 Output pin, Bypass 10μF capacitor to GND
17	FBLDO2	LDO2 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
18	LDOOUT2	LDO2 Output pin, Bypass 10μF capacitor to GND
19	VPLDO2	LDO2 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
20	ENLDO1	LDO1 Enable (Active High) or Disable(Low or Floating).
21	ENLDO2	LDO2 Enable (Active High) or Disable(Low or Floating).
22	POR	Power On Reset
23	LVEN1	LVBUCK1 Enable (Active High) or Disable(Low or Floating).
24	LVOUT1	LVBUCK1 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
25	LVVP1	LVBUCK1 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
26	LVSW1	LVBUCK1 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
27	LVGP1	Ground
28	HVOUT2	HVBUCK2 Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
29	HVBST2	Bootstrap. A capacitor connected between HVSW2 and HVBST2 pins is required to form a floating supply across the high-side switch driver. Use a 22nF capacitor
30	HVGP2	Ground
31	NC1	NC
32	HVSW2	HVBUCK2 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
33	HVVP2	HVBUCK2 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
34	HVEN2	HVBUCK2 Enable (Active High) or Disable(Low or Floating).
35	GND2	Ground
36	HVEN1	HVBUCK1 Enable (Active High) or Disable(Low or Floating).
37	HVVP1	HVBUCK1 Power supply Pin, Bypass 10μF capacitor to GND to reduce the input noise.
38	HVSW1	HVBUCK1 Switching Pin, Connect this Pin to inductor, Minimize the track area to reduce EMI.
39	NC2	NC
40	NC3	NC
41	EP	Thermal PAD, connect to Ground.

TYPICAL APPLICATIONS



SYSTEM BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNIT
HVVP1,HVSW1,HVEN1	-0.3	30	V
HVVP2,HVSW2,HVEN2	-0.3	30	V
BSTSW,BSTOUT	-0.3	30	V
HVBST1,HVBST2		HVSWX+6	V
Other pin Voltage	-0.3	10	V
Junction Temperature		125	°C
Operating Temperature	-40	125	°C
Storage Temperature Range	-55	150	°C
Lead Temperature		300	°C
Power Dissipation,P_D@T_A-25°C, QFN40L 5X5		2.5	W
HBM(Human Body Mode)		2	kV
MM(Machine Mode)		200	V

ESD(electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
HVVP1,HVSW1,HVEN1	3.4	20	V
HVVP2,HVSW2,HVEN2	3.4	20	V
BSTSW	3.4	20	V
Other pin Voltage	2.5	6	V

ELECTRICAL CHARACTERISTICS

HVBUCK1 & HVBUCK2 Electrical Characteristics

(V_{IN} = 12V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	HVVP1/2		3.4		20	V
Input UVP Threshold		Input Voltage Falling			3	V
Input OVP Threshold		Input Voltage Rising		20		V
Standby Supply Current		HVOUTX= 103% I_{OUT} = 0		400	600	μA
Shutdown Supply Current		HVENX = 0 HVVPX = 12V		3		μA
EN Rising Threshold	HVENX	HVENX RISING		1.4		V
EN Falling Threshold	HVENX	HVENX FALLING		0.6		V
Feedback Voltage	HVOUTX		0.588	0.6	0.612	V
Output Voltage Line Regulation				0.04	0.4	%/V
Output Voltage Load Regulation				0.5		%
Current Limit	I_{LIM}	Duty = 30%		3.5		A
Oscillator Frequency	F_{SW}			1.2		MHz
NMOS On Resistance	R_{ONN}	I_{SW}=100mA		0.07		Ω

LVBUCK1 & LVBUCK2 Electrical Characteristics

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	LVVP1/2		2.5		6	V

Input UVP Threshold		Input Voltage Falling		2.2		V
Input OVP Threshold		Input Voltage Rising		6.5		V
Operating Supply Current		LVOUTX = 60% I_{OUT} = 0		150	200	µA
Standby Supply Current		LVOUTX= 103% I_{OUT} = 0		40	80	µA
Shutdown Supply Current		LVENX = 0, LVVPX = 4.2V		0.1	1	µA
EN Rising Threshold	LVENX	LVENX Rising		1.4		V
EN Falling Threshold	LVENX	LVENX Falling		0.6		V
Output Voltage Regulation Accuracy			-1.5	1	1.5	%
Feedback Voltage	LVOUTX		0.588	0.6	0.612	V
Output Voltage Line Regulation				0.04	0.4	%/V
Output Voltage Load Regulation				0.5		%
Current Limit	I_{LIM}	Duty = 30%		3.5		A
Oscillator Frequency	F_{SW}			1.2		MHz
PMOS On Resistance	R_{ONP}	I_{SW}=100mA		0.1		Ω
NMOS On Resistance	R_{ONN}	I_{SW}=100mA		0.07		Ω

LDO1 & LDO2 Electrical Characteristics

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	VPLDOX		2.5		6	V
Input UVP Threshold		Input Voltage Falling		2.2	3	V
EN Rising Threshold	ENLDOX	ENLDOX Rising		1.4		V
EN Falling Threshold	ENLDOX	ENLDOX Falling		0.6		V
Output Voltage Accuracy			-3	1.5	3	%
Feedback Voltage (LDO2)	FBLDO2		0.588	0.6	0.612	V

LNB Power Supply（BOOST） Electrical Characteristics

(V_{IN} = 3.6V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V_{IN}		3.4		20	V
Input UVP Threshold		Input Voltage Falling		3		V
Operating Supply Current		Switching		0.15	0.3	mA
Quiescent Supply Current		Not Switching		50	100	µA
EN Rising Threshold	BSTEN	BSTEN Rising		1.4		V
EN Falling Threshold	BSTEN	BSTEN Falling		0.6		V
Output Voltage Accuracy			-3	1.5	3	%
Switching Frequency	F_{SW}			1.2		MHz
Maximum Duty Cycle	D_{MAX}		87	92		%
Switch Current Limit	I_{LIM}	Duty = 75%		2		A
Switch On Resistance		I_{SW} = 100mA		0.15		Ω
Switch Leakage Current		V_{SW} = 10V, V_{IN} = 3V			10	µA
Output Voltage Control	LTOH	High level voltage		1.8		V
		Low level voltage			0.4	V
Regulated output voltage	V_{OUT}	BSTEN=3.3V LTOH=0V		14.4		V
		BSTEN=3.3V LTOH=3.3V		19.4		V

RESET MONITOR Electrical Characteristics
(V_{PULLUP} = 3.3V, T_A= 25°C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POR threshold	V_{HVOUT2}	V_{HVOUT2} rising	85	90	95	%
Delay time	T_{delay}	Delay before POR released		100		ms

GENERAL DESCRIPTION

Feature Description
DF1508 is a highly efficient and integrated Power Management IC for analog and digital satellite receivers. The device incorporates 4 high-efficiency synchronous buck regulators, 1 high-efficiency asynchronous boost regulator and and 2 LDO that deliver 7 output voltages.The device also includes a reset monitor that provides a reset output signal for processor.
Each of the buck regulators is specially designed for high-efficiency operation throughout the load range. With 1.2MHz typical switching frequency, the external L- C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.
Additional features include soft-start, under-voltage lockout, over-voltage lockout, short-current protection, over-current protection and thermal overload protection. All BUCKs can operate in automatic mode (PWM/PFM). At very light loads, BUCKs enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Soft start
Each of converters has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps.
For BUCKs the soft start is implemented by increasing the switch current limit in steps that are gradually set higher. The startup time depends on the output capacitor size, load current and output voltage.

Current Limiting
A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

Startup Sequence
Once HVVP1/HVVP2/LVVP1/LVVP2/VPLOD1/VPLDO2 reaches the UVP threshold and the ENABLE pin= High the HVBUCKX/LVBUCKX/LDOX will start up.

Reset Monitor
The POR pin of DF1508 is an open-drain output between the POR pin and the GND pin. The power on reset output asserts low until the output voltage on the HVOUT2 pin exceeds the setting thresholds (91%) and the deglitch timer(100ms) has expired. Additionally, whenever the HVEN2 pin is low or open, POR immediately asserts low regardless of the output voltage.
When the POR is released (not asserted low) an external resistor connected to any external bias voltage pulls up this POR pin.

Under Voltage Protection (UVP)
HVVP1/HVVP2/LVVP1/LVVP2/VPLOD1/VPLDO2 voltage is monitored for a supply under voltage condition, for which the operation of the device cannot be guaranteed. The part will automatically disable. To prevent unstable operation, the UVP has a hysteresis window. Each under voltage protection (UVP) will disable it’s outputs, Once the supply voltage is above the UVP hysteresis, the device will initiate a power-up sequence and then enter the active state.

Over Voltage Protection (OVP)
HVVP1/HVVP2/LVVP1/LVVP2 voltage is monitored for a supply over voltage condition, for which the operation of the device cannot be guaranteed. The purpose of OVP is to protect the part and all other components connected to the PMIC outputs from any damage and malfunction. Once HVVP1/HVVP2 rises over about 20V, HVBUCK1/HVBUCK2 will be disabled automatically. To prevent unstable operation, the OVP has a hysteresis window. An over voltage protection (OVP) will force the device into the reset state, Once the supply voltage goes below the OVP lower threshold, the device will initiate a

power-up sequence and then enter the active state. HVBUCK1/HVBUCK2 operating maximum input voltage at which parameters are guaranteed is 20V. Absolute maximum of the device is30 V.

Thermal Shutdown(OTP)
The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device cannot be guaranteed. The part will automatically be disabled if the temperature is too high. The thermal shutdown (OTP) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the OTP has a hysteresis window of about 20°C. Once the temperature has decreased below the OTP hysteresis, the device will initiate a power-up sequence and then enter the active state. In the active state, the part will start up as if for the first time.

Detailed Design Procedure

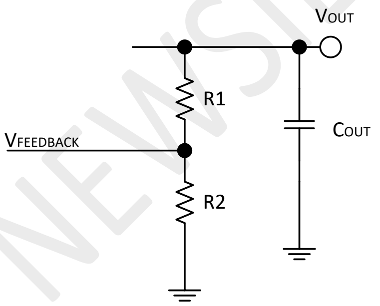
Adjusting the Output Voltage
For HVBUCK1/HVBUCK2/LVBUCK1/LVBUCK2/LDO2, A resistor divider from the output node to the feedback pin sets the output voltage. recommends using 1% tolerance or better divider resistors. Start with fixed value for the R1 resistor and use Equation to calculate R2.
To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise, and voltage errors from the feedback input current are noticeable.

$$V_{OUT}=V_{FEEDBACK}\times\frac{R1+R2}{R2}$$

Select R1 value then

$$R2=R1\times\frac{V_{FEEDBACK}}{V_{OUT}-V_{FEEDBACK}}$$

Where $V_{FEEDBACK}$=0.6V
.



BUCK Power Supply Recommendations
HVBUCK1/HVBUCK2/BOOST input voltage supply range is between 3.4 V and 20V.
LVBUCK1/LVBUCK2/LDO1/LDO2 input voltage supply range is between 2.5 V and 6V
This input supply must be well regulated. If the input supply is located more than a few inches, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47uF is a typical choice.
HVVP1/HVVP2/LVVP1/LVVP2 must all be connected to input capacitors as close as possible.

BUCK Inductor Selection
Use a 1μH-to-10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications.
For highest efficiency, select an inductor with a DC resistance less than 15mΩ. For most designs, derive the inductance value from the following equation.

$$L=\frac{V_{OUT}\times(V_{IN}-V_{OUT})}{V_{IN}\times\Delta I_L\times F_S}$$

Where ΔI_L is the inductor ripple current. Choose an inductor current approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)}=I_{LOAD}+\frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor to improve efficiency.

BUCK Input Capacitor Selection
The input current to the step-down converter is discontinuous, and therefore requires a capacitor to both supply the AC current to the step-down converter and maintain the DC input voltage. For the best performance, use low ESR capacitors, such as ceramic capacitors with X5R or X7R dielectrics and small temperature coefficients. A 22μF capacitor is sufficient for most applications. The input capacitor requires an adequate ripple current rating because it absorbs the input switching. Estimate the RMS current in the input capacitor with:

$$I_{CIN}=I_{LOAD}\times\frac{\sqrt{V_{OUT}\times(V_{IN}-V_{OUT})}}{V_{IN}}$$

The worst-case condition occurs at VIN = 2VOUT, where:

$$I_{CIN}=\frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half the maximum load current.The input capacitor can be electrolytic, tantalum,or ceramic. Place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible when using electrolytic or tantalum capacitors.When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive input voltage ripple. Estimate the input voltage ripple caused by the capacitance with:

$$\Delta V_{IN}=\frac{I_{LOAD}}{F_S\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})$$

BUCK Output Capacitor Selection

The output capacitor (C_{OUT}) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. Use low ESR capacitors to limit the output voltage ripple. Estimate the output voltage ripple with:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_S\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times\left(R_{ESR}+\frac{1}{8\times F_S\times C_{OUT}}\right)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8\times F_S^2\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with:

$$\Delta V_{OUT}=\frac{V_{OUT}}{F_S\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DF1508 can be optimized for a wide range of capacitance and ESR values.

BUCK Bootstrap Capacitor Selection

Connect a 22nF ceramic capacitor between the HVBST1/HVBST2 and HVSW1/HVSW2 pins for proper operation. recommends using a ceramic capacitor with X5R or better-grade dielectric. The capacitor should have a 6.3-V or higher voltage rating.

LDO Output Capacitor Selection

The LDO is designed to be stable with a minimum 4.7μF output capacitor. No series resistor is required when using low ESR capacitors. For most applications, a 10μF ceramic capacitor is recommended. Larger values will improve transient response, and raise the power supply rejection ratio (PSRR) of the LDO. Refer to the Typical Performance Characteristics for the allowable range of output capacitor to ensure loop stability.

LNB BOOST Inductor Selection

The inductor is required to force the higher output voltage while being driven by the input voltage. A larger value inductor results in less ripple current, resulting in lower peak inductor current and reducing stress on the internal N-Channel. MOSFET switch. However, the larger value inductor has a larger physical size,higher series resistance, and/or lower saturation current

Choose an inductor that does not saturate under the worst-case load transient and startup conditions. A good rule for determining the inductance is to allow the peak-to-peak ripple current to be approximately 30% to 50% of the maximum input current. Make sure that the peak inductor current is below 3A to prevent loss of regulation due to the current limit. Calculate the required inductance value by the equation:

$$L=\frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}\times\Delta I_L\times F_S}$$

$$I_{IN(MAX)}=\frac{V_{OUT}\times I_{LOAD(MAX)}}{V_{IN}\times\eta}$$

$$\Delta I=(30\%\sim50\%)\times I_{IN(MAX)}$$

Where V_{IN} is the input voltage, F_S is the switching frequency, $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current and η is the efficiency.

LNB BOOST Input Capacitor Selection

An input capacitor is required to supply the AC ripple current to the inductor, while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC to a minimum. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.Use an input capacitor value greater than 10μF. The capacitor can be electrolytic, tantalum or ceramic. However since it absorbs the input switching current it requires an adequate ripple current rating. Use a capacitor with RMS current rating greater than the inductor ripple current. To insure stable operation place the input capacitor as close to the IC as possible. Alternately a smaller high quality ceramic 0.1Mf capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, it is recommended that the larger capacitor be a tantalum or electrolytic type. All ceramic capacitors should be placed close to the DF1508.

LNB BOOST Output Capacitor Selection

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple to a minimum. The characteristic of the output capacitor also affects the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. In the case of ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, and so the output voltage ripple is mostly independent of the ESR. The output voltage ripple is calculated as:

$$V_{RIPPLE}=\frac{I_{LOAD}\times(V_{OUT}-V_{IN})}{V_{OUT}\times C_{OUT}\times F_S}$$

Where V_{RIPPLE} is the output ripple voltage, VIN and V_{OUT} are the DC input and output voltages respectively, I_{LOAD} is the load current, F_S is the switching frequency, and C_{OUT} is the capacitance of the output capacitor. In the case of tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency, and so the output ripple is calculated as:

$$V_{RIPPLE}=I_{LOAD}\times[\frac{(V_{OUT}-V_{IN})}{V_{OUT}\times C_{OUT}\times F_S}+\frac{R_{ESR}\times V_{OUT}}{V_{IN}}]$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. Place the output capacitor close to SW to minimize the AC loop and switching noise.

LNB BOOST Diode Selection

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. To reduce losses due to diode forward voltage and recovery time, use a Schottky diode. Choose a diode whose maximum reverse voltage rating is greater than the maximum output voltage. The rated average forward current needs to be equal to or greater than the load current.

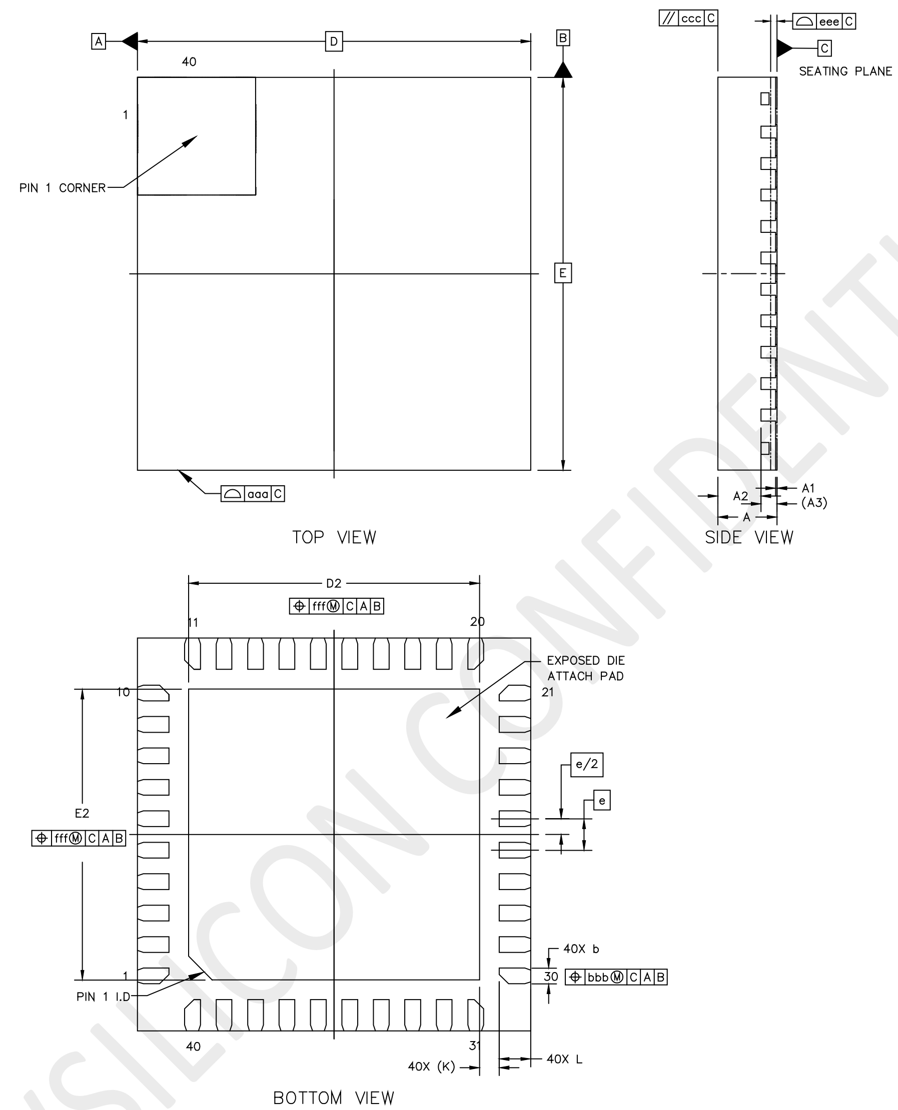
Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

PACKAGE

QFN40L_5X5



NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES;
4.FINISH: Cu/EP Sn8~20s

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	